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250+ Digital Logic Design Interview Questions and Answers, Question1: Explain about setup time and hold time, what will happen if there is setup time and hold time violation, how to overcome this? Question2: What is skew, what are problems associated with it and how to minimize it? Question3: What is slack? Question4: What is glitch?

TOP 250+ Digital Logic Design Interview Questions and ...

Logic-based interview puzzles are becoming increasingly popular in recruitment processes to help employers find the brightest candidates and gain insight into a candidate's thought process. Brain teasers are particularly popular in the tech sector, where employers want to find the most logical candidates who can help them advance with their next innovative product launch.

Logic-Based Interview Questions For Employers - Minutehack

Logical interview questions involve solving brainteasers or some type of riddle to show the interviewer your critical thinking skills, problem-solving skills and analytical skills. Logic questions for interview purposes can be used to assess these skillsets as well as

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gauge the way you ask for information, use resources and work under pressure.

10 Logical Interview Questions You Might Be Asked in an ...

Design Interview Questions 1 : Here are some Design problems that I have encountered at some point in my experience as a Designer and had discussions with others on possible solutions. Please note that there can be multiple approaches to solve the same problem so there are no exclusive right answers.

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54 Logical Interview Questions and Answers

These are some of the most commonly asked questions in digital logic design for VLSI related jobs Finite state machines mealy and moore

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machine. Sequence detection like 10100,01011 etc using both mealy and moore machine and their verilog implementation Combinational circuits like carry look ahead adder, Multiplexers, decoder, Priority encoders etc

What are Digital Logic Design interview questions? - Quora

Digital Logic Design VIVA Questions :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold time violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

400+ TOP Digital Logic Design VIVA Questions and Answers

Welcome to Interview Questions Section on FullChipDesign. Getting through interviews is always a challenging task and requires thorough preparation. Here is a list of probable questions that may appear in an interview related to RTL skills. Three areas are covered Digital Design, Digital Fundamentals and FPGA Design.

Welcome to Interview Questions Section on FullChipDesign.

9) What are the basic Logic gates? There are three basic logic gates- AND gate. OR gate. NOT gate. 10) Which gates are called as Universal

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gate and what are its advantages? The Universal gates are NAND and NOR. The advantages of these gates are that they can be used for any logic calculation. 11) What are the applications of the octal number system?

[Top 39 Digital Electronics Interview Questions - javatpoint](#)

Finally, it's an overview of digital electronics interview questions on major topics. I hope you will have good preparation after reading this 2018 digital electronics interview questions article and I will suggest practicing questions on logical gates for Interview preparation. Recommended Article

[10 Essential Digital Electronics Interview Questions ...](#)

Logic Design Engineer at Intel Corporation was asked... Oct 14, 2015. basic questions on logic design , difference between latch and flipflop, setup time ,hold time, violations and how to avoid violations,built and , or ,nand gates using MUXs. Be the first to answer this question.

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There are still more devices that we can make using a 2:1 MUX. These are some of the favorite static timing analysis and logic design

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interview questions and they are about making memory elements using the 2:1 MUX. We know the equation of a MUX is : $Out = S * A + (\overline{S}) * B$. We also know that level sensitive latch equation is. If (Clock)

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This is a collection of VLSI/ASIC digital logic design interview questions, partially documented at really taken interviews, partially designed based on the commonly asked questions and usually touched

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issues. Most of the questions relate to simplified design principles, techniques and tricks, the real-world VLSI/ASIC front-end (logic) design engineers usually use and implement in their work ...

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