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The current activities in the design of testable/fault tolerant integrated circuits are reviewed and areas for future emphasis are suggested. The rapid evolution of high performance Very Large Scale Integrated Circuits (VLSICs) has resulted in accelerated opportunities for improving the operational performance of military electronic systems. ...

The use of fault tolerant and testable high performance ...
Title: Fault Tolerant and Fault Testable Hardware ... Publisher: Prentice Hall Publication Date: 1984 Book Condition: Very Good. Top Search Results from the AbeBooks Marketplace 1. Fault-tolerant and Fault-testable Hardware Design. Parag K. Lala. Published by ...

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Fault tolerance as a property finds application in a wide variety of scenarios ranging from satellites to modern microprocessors. Fault tolerant systems have the capability of withstanding defects and are able to provide specified output despite faults occurring or having occurred. Similarly design for testability (DFT) is a technique that ...

Defect/Fault Tolerant Systems and Design for Testability ...
Students are responsible for: homework and 1-page paper summaries - 35% of grade midterm exam - 20% of grade final exam - 25% of grade individual or group project (due at beginning of class on specified day) - 20% of grade

ECE 254 / CPS 225 - Fault-Tolerant and Testable Computing ...
Objective: To provide students with an understanding of fault tolerant computers, including both the theory of how to design and evaluate them and the practical knowledge of real fault tolerant systems.

ECE/CS 554 - Fault-Tolerant and Testable Computing Systems
Another variation of this problem is when fault tolerance in one component prevents fault detection in a different component. For example, if component B performs some operation based on the output from component A, then fault tolerance in B can hide a problem with A.

Fault tolerance - Wikipedia
Fault tolerant and fault testable hardware design March 1985. March 1985. Read More. Author: Parag K. Lala. Syracuse Univ., Syracuse, NY. Publisher: Prentice-Hall, Inc. Division of Simon and Schuster One Lake Street Upper Saddle River, NJ; United States; ISBN: 978-0-13-308248-7. Available at Amazon.

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Features A systematic study of the various fault tolerant architectures in use. An in depth review of the basic characteristics of self checking logic detailed descriptions of all the major hardware techniques that may be used in fault tolerant and testable design.

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Fault tolerant and fault testable hardware design This edition published in 1985 by Prentice-Hall International in Englewood Cliffs, N.J.

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Fault-tolerant and self-testable architectures for zero failure electronics Richardson, A and Sharif, E and Betts, W R (1997) Fault-tolerant and self-testable architectures for zero failure electronics. In: AUTOMOTIVE ELECTRONICS - AUTOTECH'97. IMechE seminar publication ; 1997-10.

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Additional Physical Format: Online version: Lala, Parag K., 1948-Fault tolerant and fault testable hardware design. Englewood Cliffs, N.J. : Prentice-Hall ...

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Lala conveys concepts in a clear, informal manner, reaching abstract levels only when absolutely necessary. The objective is to not to avoid necessary theory, but to demonstrate theory through examples in order to establish the th eoretical basis for practical applications. This book presents the essentials of modern logic design, including many topics that are inadequately covered or completely ignored in other book.

With VLSI chip transistors getting smaller and smaller, today's digital systems are more complex than ever before. This increased complexity leads to more cross-talk, noise, and other sources of transient errors during normal operation. Traditional off-line testing strategies cannot guarantee detection of these transient faults. And with critical applications relying on faster, more powerful chips, fault-tolerant, self-checking mechanisms must be built in to assure reliable operation. Self-Checking and Fault-Tolerant Digital Design deals extensively with self-checking design techniques and is the only book that emphasizes major techniques for hardware fault tolerance. Graduate students in VLSI design courses as well as practicing designers will appreciate this balanced treatment of the concepts and theory underlying fault tolerance along with the practical techniques used to create fault-tolerant systems. Features: Introduces reliability theory and the importance of maintainability Presents coding and the construction of several error detecting and correcting codes Discusses in depth, the available techniques for fail-safe design of combinational circuits Details checker design techniques for detecting erroneous bits and encoding output of self-checking circuits Demonstrates how to design self-checking sequential circuits, including a technique for fail-safe state machine design

For the editors of this book, as well as for many other researchers in the area of fault-tolerant computing, Dr. William Caswell Carter is one of the key figures in the formation and development of this important field. We felt that the IFIP Working Group 10.4 at Baden, Austria, in June 1986, which coincided with an important step in Bill's career, was an appropriate occasion to honor Bill's contributions and achievements by organizing a one day "Symposium on the Evolution of Fault-Tolerant Computing" in the honor of William C. Carter. The Symposium, held on June 30, 1986, brought together a group of eminent scientists from all over the world to discuss the evolu tion, the state of the art, and the future perspectives of the field of fault-tolerant computing. Historic developments in academia and industry were presented by individuals who themselves have actively been involved in bringing them about. The Symposium proved to be a unique historic event and these Proceedings, which contain the final versions of the papers presented at Baden, are an authentic reference document.

This book deals with primarily with reliable and faul-tolerant circuit design and evaluation techniques for RAMS. It examines both the manufacturing faul-tolerance (e.g. self-repair at the time of manufacturing) and online and field-related fault-tolerance (e.g. error-correction). It talks a lot about important techniques and requirements, and explains what needs to be done and why for each of the techniques.

Fault-Tolerant Systems is the first book on fault tolerance design with a systems approach to both hardware and software. No other text on the market takes this approach, nor offers the comprehensive and up-to-date treatment that Koren and Krishna provide. This book incorporates case studies that highlight six different computer systems with fault-tolerance techniques implemented in their design. A complete ancillary package is available to lecturers, including online solutions manual for instructors and PowerPoint slides. Students, designers, and architects of high performance processors will value this comprehensive overview of the field. The first book on fault tolerance design with a systems approach Comprehensive coverage of both hardware and software fault tolerance, as well as information and time redundancy Incorporated case studies highlight six different computer systems with fault-tolerance techniques implemented in their design Available to lecturers is a complete ancillary package including online solutions manual for instructors and PowerPoint slides

This textbook serves as an introduction to fault-tolerance, intended for upper-division undergraduate students, graduate-level students and practicing engineers in need of an overview of the field. Readers will develop skills in modeling and evaluating fault-tolerant architectures in terms of reliability, availability and safety. They will gain a thorough understanding of fault tolerant computers, including both the theory of how to design and evaluate them and the practical knowledge of achieving fault-tolerance in electronic, communication and software systems. Coverage includes fault-tolerance techniques through hardware, software, information and time redundancy. The content is designed to be highly accessible, including numerous examples and exercises. Solutions and powerpoint slides are available for instructors.